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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/148,606

09/04/1998

KIYOSHI YONEDA

5586D-6885

3618

26021

7590

05/05/2006

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EXAMINER

LIANG, REGINA

ART UNIT

PAPER NUMBER

2629

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/148,606	Applicant(s) YONEDA ET AL.	
	Examiner Regina Liang	Art Unit 2629	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                                       | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

### DETAILED ACTION

1. This Office Action is responsive to amendment filed 3/13/06. Claims 1-27 are pending in this application.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

### *Claim Rejections - 35 USC § 103*

3. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (Figs. 1-3, page 1, line 13 to page 9, line 11) in view of Higashi (US. PAT. NO. 6,136,632).

As to claims 1, 3, Figs. 1 and 2 of the admitted prior art discloses a semiconductor device in which a plurality of semiconductor elements (sampling TFTs of drain driver, pixel TFTs in the pixel area) are formed on a substrate, wherein in at least semiconductor elements (sampling TFT 46 of the drain driver 44), among the plurality of semiconductor elements, that samples data to be supplied to other semiconductor elements (pixel TFTs), a channel width of a channel region formed in a semiconductor layer to which laser annealing is applied is larger than a channel length thereof (page 6, lines 15-20 of the specification), and Fig. 2 of the admitted prior art teaches in at least the semiconductor elements (sampling TFT 46 of the drain driver 44), among the plurality of semiconductor elements, that are connected to a signal line (drain electrode 57) to which data to be supplied to a drain of a corresponding one of the plurality of semiconductor elements (pixel TFTs) is input and which common to the plurality of semiconductor elements and that output data from the signal line, a channel width of a channel region is larger than a channel length thereof (page 6, lines 15-20 of the specification).

The admitted prior art does not disclose a channel width direction is neither vertical to nor parallel with regard to a side direction of the substrate, and the channel width direction is neither parallel with nor orthogonal to a primary direction of extension of the signal line. However, Higashi teaches an active matrix display having data driver section 7 which has n-type and p-type TFTs (at least semiconductor elements, this corresponds to sampling TFT of drain driver), wherein the transistor TFTs of the data driver section (7) are not aligned in the X or Y direction (the channel width direction is not aligned in X or Y direction, see col. 6, lines 29-35; col. 8, lines 34-39; col. 16, lines 29-33; col. 19, lines 16-19 for example). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the admitted prior art to have the channel width direction is neither vertical to nor parallel with regard to a side direction of the substrate and the channel width direction is neither parallel with nor orthogonal to a primary direction of extension of the signal line as taught by Higashi since this allows a substantial reduction in the nonuniformity in the polysilicon film, whereby a semiconductor film formed on a substrate can be uniformly crystallized by means of irradiation of a laser beam while achieving high throughput.

As to claims 2, 4, 8, 13, 19, Higashi teaches laser annealing is performed to polycrystallize an amorphous semiconductor layer and obtain a polycrystalline semiconductor layer.

As to claims 5, 10, 15, note the discussion of claim 1 above. The admitted prior art teaches the display device having a plurality of first thin-film transistors (pixel TFTs), a plurality of second thin-film transistors (sampling TFTs of drain driver).

As to claims 6, 7, 11, 12, 16, the admitted prior art teaches the second thin-film transistors (sampling TFT of the drain driver) in which the channel width is larger than the

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channel length, and Higashi teaches the second thin-film transistors (sampling TFTs) having the channel width direction is form in a direction different from the direction of the substrate (the sampling TFTs are not aligned in the X or Y direction).

As to claims 9, 14, note the discussion of claim 1 above. The admitted prior art as modified by Higashi does not explicitly disclose the second thin-film transistors (sampling TFTs) is set to a direction of about  $45^{\circ}$  relative to any one or all of a plurality of side direction of the substrate. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the admitted prior art as modified by Higashi to have the second thin-film transistors (sampling TFTs of the drain driver) to be set to a direction as claimed, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

As to claims 17, 18, 21, 22, note the discussion of claim 1 above. The admitted prior art teaches the display device having a plurality of first thin-film transistors (pixel TFTs), a plurality of second thin-film transistors (sampling TFTs of drain driver). Higashi teaches the first thin-film transistors (pixel TFTs 10) are aligned in the X and Y direction; the second thin-film transistors (sampling TFTs) are not aligned in the X and Y direction. Thus, the admitted prior art as modified by Higashi teaches the first thin-film transistors are not aligned with the direction of the first thin-film transistors, which reads on a channel width direction of some or all of second thin-film transistors being forming non-parallel with and non-orthogonal to a channel width direction of the first thin-film transistors and the channel width direction is neither parallel with nor orthogonal to a primary direction of extension of the video signal line as claimed.

As to claim 20, note the discussion of claims 1, 9 and 17 above.

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As to claims 23-27, Fig. 2 of the admitted prior art teaches a data line, the second thin-film transistors are connected to the video signal line and output display data from the video signal line to a corresponding one of the first thin-film transistors.

***Response to Arguments***

4. Applicant's arguments filed 3/13/06 have been fully considered but they are not persuasive.

Applicant's remarks regarding Applicants' admitted prior art and Higashi on pages 19-21 are not persuasive. Applicants' admitted prior art teaches the data driver circuit are formed by a TFT array of CMOS, the channel regions of the TFTs is elongated in which the channel width is larger than the channel length. Higashi teaches the data driver section 7 includes TFTs which are not aligned in the X or Y direction. For example, col. 6, lines 30-35 of Higashi teaches "in the data driver section 7 there are a great number of circuit elements, for example, a CMOS circuit such as a 2-stage inverter including, as shown in Fig. 1(B), n-type TFTs n1 and n2 and p-type TFTs p1 and p2 are **not aligned in the X and Y direction**", also col. 19, lines 16-19 of Higashi teaches "although the TFTs 10 in the active matrix section 9 are aligned in straight lines in both X and Y direction, the TFTs 10 in the data driver sections 7 are **not aligned** in straight lines". Clearly, Higashi teaches the channel width direction (TFTs in the data driver section) is aligned in a direction which is neither vertical to nor parallel with either the X or the Y direction as claimed.

***Conclusion***

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

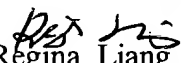
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A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Regina Liang  
Primary Examiner  
Art Unit 2674

5/3/06